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Micro-fabrication process for small transport devices of layered manganite

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Devices have been fabricated based on the bilayer manganite $La_{1.4}Sr_{1.6}Mn_2O_7$, which in the bulk state orders magnetically below 90 K, at which point both in-plane and c-axis bulk resistivity decrease by 2-3 orders of magnitude. We provide an optimized procedure to fabricate devices to electrical transport in- and out of plane. Fabricated mesoscopic devices have dimensions comparable to a typical magnetic domain, allowing us to study structures going from a single domain to several domains. © *2012 American Institute of Physics*. [doi:10.1063/1.3675995]

Materials exhibiting strong electron correlations display a wide variety of complex transport phenomena, which hold potential for increased electronic functionality complementing conventional metals and semiconductors.[1] Among the transition metal oxides, for instance, the manganites exhibit colossal magnetoresistance (CMR), which can be utilized in magnetoelectric devices. Such correlated electron technology poses three challenges: (1) Understanding bulk properties, (2) exploring how these properties are modified and eventually controlled in meso and nano-scaled structures, and (3) establishing optimal micro-fabrication process, which often requires different solutions than the well-established techniques for conventional semiconductors. The present research is aimed to study the mechanism of c-axis and in-plane charge transport in the double-layer perovskite-type manganite $La_{1.4}Sr_{1.6}Mn_2O_7$ (LSMO). In the bulk state, LSMO display highly anisotropic transport with c-axis resistivity about 3 orders of magnitude higher than the in-plane resistivity. The transition to a magnetically ordered state below 90 K is accompanied by a 2 order of magnitude drop in both in-plane and c-axis resistivity.[1–3] It has been speculated that magnetic domain walls both influence the in-plane resistivity and is responsible for the c-axis resistivity mimicking the in-plane transport.[4] It is therefore desirable to manufacture and measure electrical transport in devices on length scales comparable to typical magnetic domain sizes, which is in the micron range.[5]

To investigate, respectively, in-plane and out-of-plane resistivity, two types of devices are manufactured: (a) For measuring electrical transport along the c-axis, a trench is etched into the LSMO surface (with c-axis along the surface normal), thereby creating an island.[6] Creating two such neighboring islands with electrical contacts on top allow a 2-point measurement, whose resistivity will be dominated by the c-axis transport through the islands. (b) To characterize in-plane transport, devices with four metal contacts on a row (for four-probe measurement) on the LSMO surface are prepared. Due to the large anisotropy, the resistivity of such a device will be dominated by the in-plane resistivity, albeit there will of course be a mixing-in of the c-axis conductance, which determines how deep into the material the current will flow. This mixing is a function of device geometry and the ratio of the anisotropic resistivities and can be modeled by finite element methods.

Here, we report the fabrication process steps to manufacture devices for ab-plane measurement. Bilayer LSMO ($x = 0.3$) crystals were grown by floating zone method. The magnetic properties, which are very sensitive to doping level, measured on our crystals, are consistent with reported bulk measurements.[1,7–9] LSMO ($x = 0.3$) is cleavable[10] along (001) plane but the obtained up to micron sized terraces are not wide enough to be suitable for micro-fabrication. Therefore, crystals are cut and subsequently polished. LSMO crystals were cut by a tungsten wire saw. One side was polished and attached with less than 10 μm thick M-bond 610 glue on 1 cm × 1 cm silicon chip with 270 nm silicon oxide on top as substrate. The second side was then polished down to 100 μm thickness, achieving surface roughness less than 1 nm (Fig. 1). Polishing was performed by a Logitech PM5 polishing machine with Polytron plate. Both sides of the cut LSMO crystal was polished by use of 9 μm Al_2O_3 powder for primary thinning process down to 100 μm and afterwards SiO_2 suspension with 0.1 μm particles in pH = 9 were used for final surface polishing. The subsequent fabrication steps are sketched in Fig. 2. After polishing the LSMO surface, 10 nm Al_2O_3 was deposited by ALD (Atomic Layer Deposition) as an insulating layer. ALD was carried out in 200 °C by using trimethylaluminum (TMA) and water vapor as precursors. Both precursors stay in room temperature with pressure of 8.9 Torr for TMA and 20 Torr for water vapor. Each deposition cycle performed by one pulse TMA and 2 pulses for

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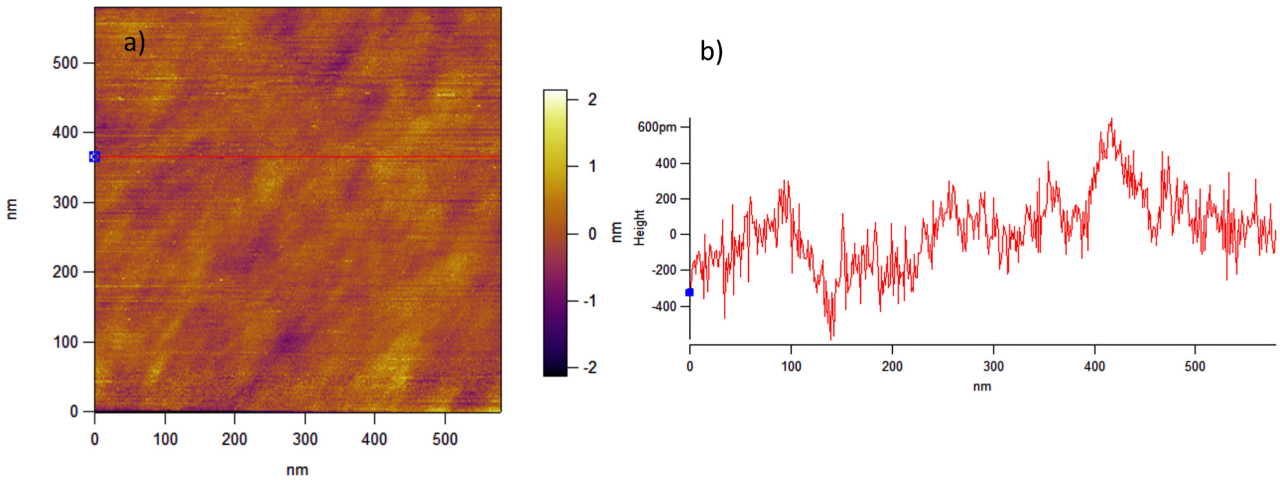

FIG. 1. (Color online) (a) AFM image of the polished $La_{1.4}Sr_{1.6}Mn_2O_7$ surface. The Horizontal line marks the line-scan shown in (b). The surface has root-mean-square roughness of 0.3 nm with 1.2 nm from peak to peak in the line profile.

water vapor that have been set to one second duration, followed by 5 s purging time for TMA and 10 s for water vapor. This cycle results in growth of 1.6 Å Al_2O_3 on the surface as the reactor pressure was kept at 90 mTorr. In the next step, the surface is covered by a layer of positive resist (300 nm PMMA (Poly(methyl methacrylate) as positive e-beam resist)), which is patterned using electron beam lithography to expose the areas, which should have contacts on LSMO. The electron beam lithography is carried out with a Vistec EBPG5000 with 100 KeV thermal field emission gun and high resolution Gaussian beam system. In the lithography process, due to different rate of electron scattering from the LSMO surface, the exposure parameters are different comparing to that for SiO_2 wafers. In this process, for the small

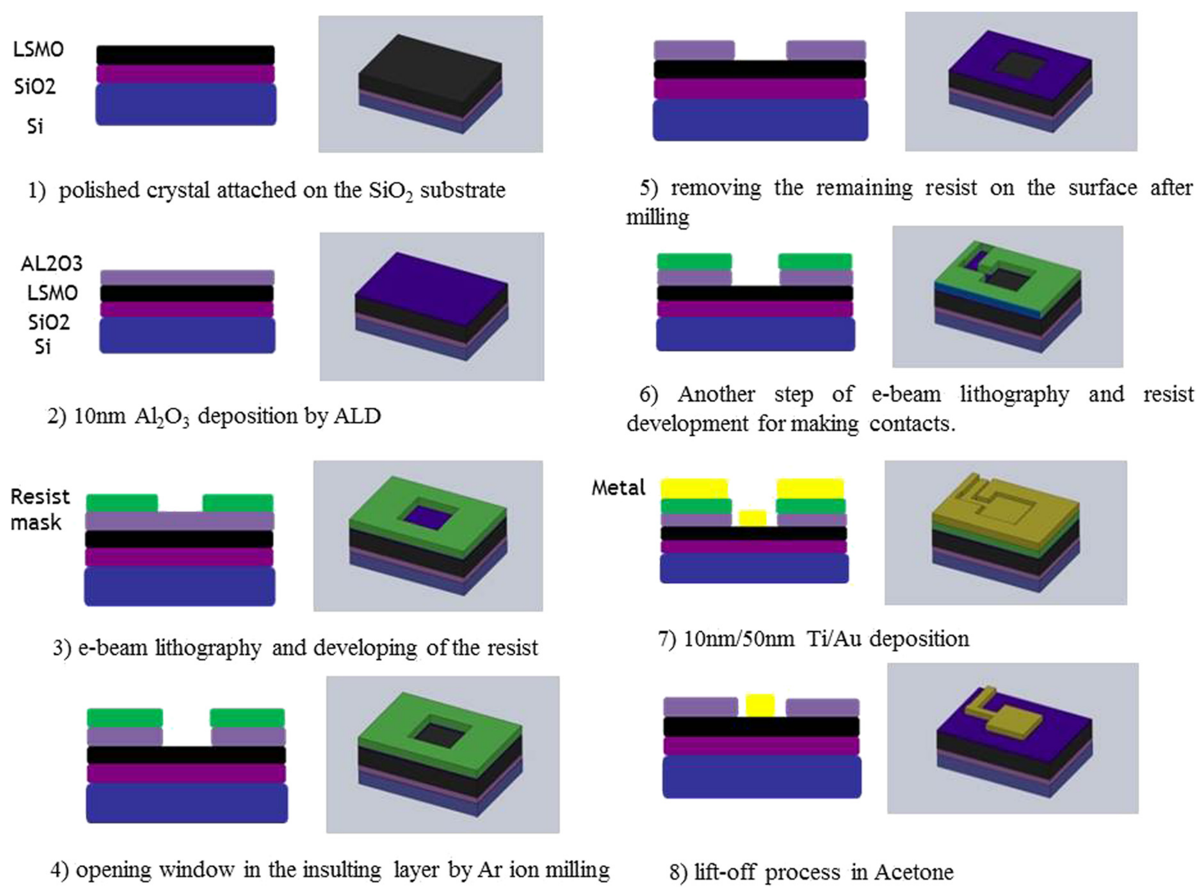

FIG. 2. (Color online) Schematic device fabrication process' steps, as described in the text. (1) Polished crystal attached on the SiO_2 substrate. (2) 10 nm Al_2O_3 deposition by ALD. (3) e-beam lithography and developing of the resist. (4) Opening window in the insulting layer by Ar ion milling. (5) Removing the remaining resist on the surface after milling. (6) Another step of e-beam lithography and resist development for making contacts. (7) 10 nm/50 nm Ti/Au deposition. (8) Lift-off process in acetone.

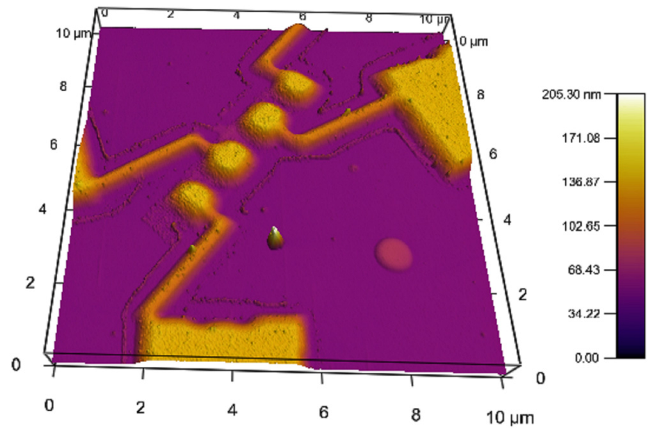

FIG. 3. (Color online) AFM image of a fabricated device with four contacts on the (001) plane of LSMO.

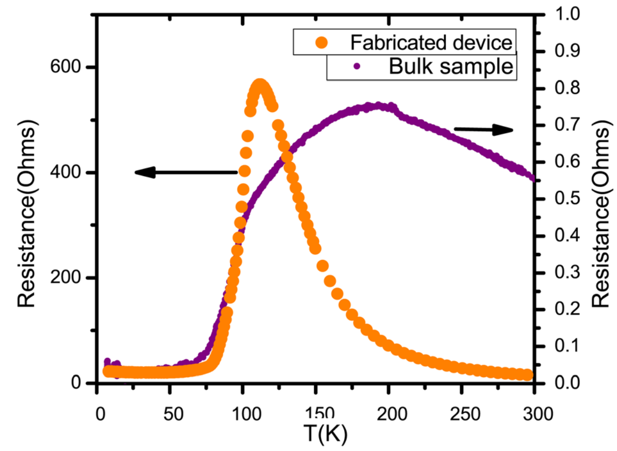

FIG. 4. (Color online) Resistance vs temperature curves for sample shown in Fig. 3 (orange), and bulk LSMO with $3 \times 3 \times 0.3$ mm^3 (purple).

parts of the designed pattern (up to few microns) 1 nA electron beam current is used with 300 μm aperture, 1200 $\frac{\mu C}{cm^2}$ as exposure dose and 5 nm for the pattern resolution. The PMMA serves as etching mask for the Argon ion milling process to etch away the 10 nm Al_2O_3 in the windows opened by electron beam lithography. As dry etching step, Alcatel AMS 200 DSE dry etcher is used for Ar ion milling. To avoid burning the positive resist used as mask and keep it solvable in acetone, during etching process the sample kept in 0 °C and a discontinuous etching process is performed, as the sample is exposed to plasma 7 times for period of 5 s.

Previously, other materials were tested as insulating layer like a layer (about 300 nm) of lift-off resist (LOR) or a layer of SiO_2 deposited by sputtering. The advantage in use of LOR would be avoiding the etching step but the exposed layer of LOR in the lithography process is not resistive to acetone and at the final step, the deposited layer of metal will be removed during the lift-off process in acetone. Also a thin layer of insulator is recommended to avoid long etching time, which can burn the resist. ALD deposited Al_2O_3 is chosen because for thin layers of about 10 nm, sputtering a thin layer of SiO2 is less precise than ALD deposition.

Another electron beam lithography step is carried out to make metal contacts on LSMO. To avoid Schottky barriers on the metal and hole doped P-type LSMO interface, the choices would be gold or platinum due to their higher work functions, but these metals are not sticky enough on LSMO and Al_2O_3 to withstand the low temperature measurements. The best solution was found to be using an intermediate layer of nonmagnetic metal like titanium. A representative fabricated device is shown in Fig. 3.

Resistivity and I-V characteristics were measured as a function of temperature using a Keithley 2400 source meter, and a homemade transport insert for a Quantum Design MPMS superconducting quantum interference device (SQUID) system, which is used for temperature control between 2 K and room temperature and allows applied fields up to 5 T. Figure 4 shows resistivity as function of temperature R(T) of the device depicted in Fig. 3, compared to the resistivity obtained from a macroscopic bulk measurement. Both curves display a drop in resistivity below the magnetic ordering temperature T_c. However, above T_c the micron sized device reveals a very different behavior. While further investigations and theoretical considerations are called for to understand the origin of this observation, it clearly demonstrates that micron sized devices capture different transport characteristics, which on one hand may be used technologically, while on the other hand may provide new insight into the complex transport mechanisms in the manganite materials.

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